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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/697,777	10/30/2003	Sonya Gary	99-LM-168C1	8897

30429 7590 05/18/2004

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EXAMINER	
VU, TRISHA U	

ART UNIT	PAPER NUMBER
2112	

DATE MAILED: 05/18/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/697,777	GARY ET AL.	
	Examiner	Art Unit	
	Trisha U. Vu	2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *20031030*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-30 are presented for examination.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 27 and 29 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

a. Claim 27 recites the limitation "the plurality of processors" in line 2. There is insufficient antecedent basis for this limitation in the claim.

b. Claim 29 recites the limitation "the controller of claim 28" in line 1. There is insufficient antecedent basis for this limitation in the claim.

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

3. Claims 1-2, 4-12, and 20-29 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-2, 4-6, 8-9, 11-13, and 17-18 of U.S. Patent No. 6,662,253.

The claims correspond to one another as follows:

Application	Patent
1	1 or 17
2	2
4	4
5	5
6	6
7	1
8	8
9	9
10	11
11	12
12	13
20	17
21	17
22	18
23	17
24	2
25	18
26	18
27	8
28	18
29	4

Although the conflicting claims are not identical, they are not patentably distinct from each other because the minor differences in the claims would have been obvious. The only different is that the corresponding patent claim is claiming a disk drive controller, and the application is an embedded computing system (as in claim 1) and a

controller (as in claim 9). It is obvious that a disk drive controller is an example of an embedded system and a controller.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-2, 5, 7-8, and 25-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tanaka (5,408,671) in view of Stirk et al. (5,408,627) (hereinafter Stirk) and further in view of Starke (5,889,947).

As to claim 1, Tanaka disclose a computing system comprising: a plurality of processors; a bus coupling to a plurality of peripheral units (registers) (Fig. 1); coupling each of the plurality of processors to the bus in response to an owner signal (through access control means 16); a set of peripheral-share registers (shared register control portion) wherein each member of the set includes an entry associated with each of the plurality of peripheral units holding a state value indicating which of the plurality of processors currently owns the associated peripheral unit (note col. 1, lines 50-65). However, Tanaka does not explicitly disclose a multiplexor for coupling each of the plurality of processors to the bus. Stirk teaches multiplexor circuit (Data MUX 46, Address MUX 50, and associated circuits) for coupling each of the plurality of processors

(A, B, C) to the bus (Figs. 3A-3B and col. 2 line 57 to col. 3 line 44). It would have been obvious to one of ordinary skill in the art at the time the invention was made to include the multiplexor circuitry for coupling each of the plurality of processor to the bus as taught by Stirk in the system of Tanaka to provide efficient accessing to a share resource by a plurality of processors with a low cost (col. 1, lines 13-52) and also to minimize access contention for frequently access of a processor to a particular peripheral unit (by arbitration unit 52). However, Tanaka and Stirk do not explicitly disclose the computing system is embedded system. Starke teaches implementing the system as embedded system (col. 4, lines 32-57). It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the system of Tanaka and Stirk to be embedded system as taught by Starke to provide greatly increased data bandwidth and decreased latency (col. 3, lines 53-63).

As to claim 2, Stirk further teaches the multiplexor is bi-directional (note at least col. 4 line 59 to col. 5 line 9 wherein the multiplexor circuitry allows communication from the processor to the memory and from memory to the processor) and comprises: an address multiplexor (MUX 50) coupled to address outputs of each of the plurality of processors wherein the address multiplexor selectively couples one of the processor address outputs to a MUX address output based on the state of the owner signal (MUX_SEL); a data multiplexor (MUX 46) coupled to data outputs of each of the plurality of processors, wherein the data multiplexor selectively couples one of the processor data outputs to a MUX data output based on the state of the owner signal (MUX_SEL); and a shared register (memory interface logic 38) having an address port

coupled to the MUX address output, a data port coupled to the MUX data output, and a bus port coupled to communicate with the bus (to the memory 24) (Figs. 3A-3B).

As to claim 5, Tanaka further teaches the set peripheral share registers includes a plurality of release registers (M1 through M4) such that each release register corresponds to one of the plurality of processors (processors P1 through P4), wherein each release register has an entry associated with each of the peripheral units, and wherein each entry holds a value indicating whether the corresponding processor is releasing ownership of the associated peripheral unit (note col3, lines 65-68 wherein the bit value of 1 indicates that the shared register is used by the processor and the bit value of 0 indicates that the shared register is not used (released) by the processor).

As to claim 7, Tanaka further teaches the system further comprises the peripheral units and wherein the processors and the peripheral units comprise a single integrated circuit (as modified above by Starke to implement the system in a single integrated circuit) (Starke, col. 4, lines 32-57).

As to claim 8, Tanaka further teaches the state value is dynamically configurable during operation by at least one of the plurality of processors (note col. 4, lines 33-66).

As to claim 25, Tanaka teaches a multiprocessor system comprising: a pair of processors; a plurality of peripheral units (registers) (Fig. 1); a bus coupling to each of the peripheral units (Fig. 1). However, Tanaka does not explicitly disclose a multiplexor for selectively coupling each of processors to the bus in response to an owner signal. Stirk teaches multiplexor circuit (Data MUX 46, Address MUX 50, and associated circuits) for coupling each of the plurality of processors (A, B, C) to the bus in response to an owner

signal (MUX_SEL) (Figs. 3A-3B and col. 2 line 57 to col. 3 line 44). It would have been obvious to one of ordinary skill in the art at the time the invention was made to include the multiplexor circuitry for coupling each of the processor to the bus as taught by Stirk in the system of Tanaka to provide efficient accessing to a share resource by a plurality of processors with a low cost (col. 1, lines 13-52) and also to minimize access contention for frequently access of a processor to a particular peripheral unit (by arbitration unit 52). However, Tanaka and Stirk do not explicitly disclose the peripheral units, the processors, and the multiplexor comprise a single integrated circuit. Starke teaches implementing the system as a single integrated circuit (col. 4, lines 32-57). It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the system to be a single integrated circuit as taught by Starke in the system of Tanaka and Stirk to provide greatly increased data bandwidth and decreased latency (col. 3, lines 53-63).

As to claim 26, Tanaka further teaches a set of peripheral-share registers (in shared register control portion) including an entry associated with each of the peripheral units holding a state value indicating which one of the processors currently owns the associated peripheral unit (Fig.1, col. 1, lines 50-65, and col. 3, liens 23-68).

As to claim 27, Tanaka further teaches the state value is dynamically configurable during operation by at least one of the processors (note col. 4, lines 33-66).

As to claim 28, Stirk further teaches the multiplexor is bi-directional (note at least col. 4 line 59 to col. 5 line 9 wherein the multiplexor circuitry allows communication from the processor to the memory and from memory to the processor) and comprises: an

address multiplexor (MUX 50) coupled to address outputs of each of the processors wherein the address multiplexor selectively couples one of the processor address outputs to a MUX address output based on the state of the owner signal (MUX_SEL); a data multiplexor (MUX 46) coupled to data outputs of each of the processors, wherein the data multiplexor selectively couples one of the processor data outputs to a MUX data output based on the state of the owner signal (MUX_SEL); and a shared register (memory interface logic 38) having an address port coupled to the MUX address output, a data port coupled to the MUX data output, and a bus port coupled to communicate with the bus (to the memory 24) (Figs. 3A-3B).

5. Claims 3 and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tanaka (5,408,671) in view of Stirk et al. (5,408,627) (hereinafter Stirk) and Starke (5,889,947), and further in view of Gorishek, IV et al. (6,480,952) (hereinafter Gorishek).

As to claims 3 and 30, the argument above for claims 1 and 25 applies. However, Tanaka, Stirk, and Starke do not explicitly disclose one of the processors is dedicated to executing operating system code and another one of the processors is executing application code. Gorishek teaches multiprocessing system in which one of the processors is dedicated to executing operating system code and another one of the processors is executing application code (col. 4, lines 23-54). It would have been obvious to one of ordinary skill in the art at the time the invention was made to include executing operating system code by one of the processors and executing application code by another one of the processors as taught by Gorishek in the system of Tanaka, Stirk,

and Starke to provide greater performance and greater number of application programs executable by the computer system (col. 22, lines 8-23).

6. Claims 4 and 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over by Tanaka (5,408,671) in view of Stirk et al. (5,408,627) (hereinafter Stirk) and Starke (5,889,947), and further in view of Dahlen (5,317,749).

As to claims 4 and 29, the argument above for claim 1 and 28 applies. Tanaka further teaches the set of peripheral share registers includes a plurality of registers (M1 through M4) such that each register corresponds to one of the plurality of processors (processors P1 through P4), wherein each register has an entry associated with each of the peripheral units, and wherein each entry holds a value indicating whether the corresponding processor is currently using the associated peripheral unit (note col. 3, lines 65-68). However, Tanaka, Stirk, and Starke do not explicitly disclose indication whether the corresponding processor is requesting ownership of the associated peripheral unit. Dahlen teaches indication of whether a processor is requesting ownership of a peripheral unit (waiting for shared access to the resource) (note col. 3, lines 60-63). It would have been obvious to one of ordinary skill in the art at the time the invention was made to include indication of whether a processor is requesting ownership of a peripheral unit as suggested by Dahlen using the registers (M1 through M4) implementation of Tanaka such that each register corresponds to one of the plurality of processors wherein each register has an entry associated with each of the peripheral units in the system of

Tanaka, Stirk, and Starke to prevent any processor which has submitted an access request from being "locked out" (note col. 3, lines 4-18).

7. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tanaka (5,408,671) in view of Stirk et al. (5,408,627) (hereinafter Stirk) and Starke (5,889,947), and further in view of Vartti et al. (5,678,026) (herein after Vartti).

As to claim 6, the argument above for claim 1 applies. Tanaka further teaches shared registers having an entry associated with each of the peripheral units, wherein each entry holds a value indicating the shared register used by each processor (note col. 3, lines 65-68). However, Tanaka, Stirk, and Starke do not explicitly disclose indicating which of the plurality of processors wins ownership of the associated peripheral unit when a conflict occurs between two or more of the processors requesting ownership of the associated peripheral unit. Vartti teaches, associated with each of the peripheral unit, indicating which of the plurality of processors (local/remote requesters wherein local requester has priority) wins ownership of the associated peripheral unit when a conflict occurs between two or more of the processors requesting ownership of the associated peripheral unit (trying to lock the same address at the same time) (note col. 13, lines 36-67 and col. 14, lines 1-27). It would have been obvious to one of ordinary skill in the art at the time the invention was made to include associated with each of the peripheral unit, indicating which of the plurality of processors wins ownership of the associated peripheral unit when a conflict occurs between two or more of the processors requesting ownership of the associated peripheral unit as suggested by Vartti in the system of

Tanaka, Stirk, and Starke to minimize priority contention for frequently access of a processor to a particular peripheral unit.

8. Claims 9-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dahlen (5,317,749) in view of Lehman et al. (4,796,179) (hereinafter Lehman).

As to claim 9, Dahlen teaches a method for sharing a plurality of peripheral units (resources) in a multiprocessor system having a plurality of processors (note col. 1, lines 7-10) comprising: generating a plurality of access requests using the plurality of processors (note col. 3, lines 4-6); storing a state value associated with each peripheral unit, the state value indicating which of the plurality of processors is a current owner of the associated peripheral (note col. 3, lines 63-68 and col. 4, lines 1-2); and selectively coupling each peripheral unit to receive only access requests generated by a particular processor indicated by the state value associated with that peripheral unit (note col. 7, lines 1-7). However, Dahlen does not explicitly disclose the plurality of processors in a controller. Lehman teaches multiprocessor controller (col. 38, lines 23-30). It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement multiprocessor controller as taught by Lehman in the system of Dahlen to allow more than one set of computations to be performed at a time (col. 38, lines 23-30).

As to claim 10, Dahlen further teaches dynamically altering the state values to create dynamic ownership associations between a peripheral and the plurality of processors (note col. 2, lines 33-38, col. 9, lines 56-68 and col. 10, lines 1-4 wherein the bit value associated with each processor owning the resource is reset for each access).

As to claim 11, Dahlen further teaches providing a request register for each processor (note col. 3, line 68 and col. 4, lines 1-2); providing a release register (note col. 9, lines 64-68 wherein the latch control word is zeroed out if the processor is giving up exclusive control); in response to receiving a request for access to a specified peripheral from a first processor, generating an indication in the request register that that the first processor has a pending access request; determining from the state value whether any processor other than the first processor is the current owner of the specified peripheral; when a second processor owns the peripheral, holding the request in a pending state (note col. 2, lines 45-53); generating an indication in the release register in indicating that the second processor is releasing ownership of the peripheral; and in response to the indication in the release register, clearing both the request indication and the release indication and hanging the state value to indicate that the first processor is the current owner of the specified peripheral (note col. 2, lines 33-44).

As to claim 12, Dahlen further teaches the step of providing a request register comprises implementing a data structure for each processor, where each data structure comprises a plurality of entries and each of the entries is associated with a specific one of the plurality of peripheral units, and the step of providing a release register comprises implementing a data structure for each processor, where each data structure comprises a plurality of entries and each of the entries is associated with a specific one of the plurality of peripheral units (note col. 3, lines 65-68 and col. 4, lines 1-2).

9. Claims 13-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tanaka (5,408,671), in view of Stirk et al. (5,408,627) (hereinafter Stirk), in view of Starke (5,889,947), and further in view of Lehman et al. (4,796,179) (hereinafter Lehman).

As to claim 13, Tanaka teaches a multiprocessor system comprising: first and second processors; a plurality of peripherals (registers) (Fig. 1); a bus coupling the processors to the peripherals (Fig. 1); and each of the peripherals is only used by one of the processors at a particular time (note col. 1, lines 50-65). However, Tanaka does not explicitly disclose means for arbitrating between the processors for communication access to requested ones of the peripherals wherein the arbitrating means comprises logic for determining which of the processors is an owner of a requested one of the peripherals. Stirk teaches means for arbitrating (arbitration 52 and associated circuit) between the processors for communication access to a requested peripheral wherein the arbitrating means comprises logic for determining which of the processors is an owner of the requested peripheral (Figs. 3A-3B and col. 3, lines 1-36). It would have been obvious to one of ordinary skill in the art at the time the invention was made to include the arbitrating circuitry as taught by Stirk in the system of Tanaka to minimize access contention for frequently access of a processor to a particular peripheral unit. However, Tanaka and Stirk do not explicitly disclose the processors being processor cores. Starke teaches processor cores integrated on a single integrated circuit chip (col. 3, lines 53-63 and col. 4, lines 32-57). It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement processor cores as taught by Starke in the system of Tanaka and Stirk to provide greatly increased data bandwidth and decreased

latency (col. 3, lines 53-63). However, Tanaka, Stirk, and Starke do not explicitly disclose multiprocessor system being a multiprocessor controller. Lehman teaches multiprocessor controller comprising a plurality of processors (col. 38, lines 23-30). It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement multiprocessor controller as taught by Lehman in the system of Tanaka, Stirk, and Starke to allow more than one set of computations to be performed at a time (col. 38, lines 23-30).

As to claim 14, Stirk further teaches the bus comprises an address bus and a data bus for each of the processor cores (Figs. 3A-3B).

As to claim 15, Stirk further teaches the arbitrating means further comprises a multiplexor (Data MUX 46, Address MUX 50, and associated circuits) for selecting the address and data buses corresponding to one of the core processors (A, B, C) to the bus in response to an owner signal corresponding to the ownership determination (Figs. 3A-3B and col. 2 line 57 to col. 3 line 44).

As to claim 16, Tanaka further teaches a control register for each of the peripherals storing an ownership state indicating which of the core processors controls ownership (note col. 3, lines 23-43).

As to claim 17, Tanaka further teaches a set of peripheral-share registers (in shared register control portion 1) wherein a first member of the set includes an entry associated with each of the plurality of peripheral units that holds a state value indicating which of the processor cores currently owns the associated peripheral (note col. 3, lines 23-43). Stirk further teaches the arbitrating means further comprises a multiplexor for

selectable coupling the processor cores to the bus in response to an owner signal, the multiplexor comprising: an address multiplexor (MUX 50) coupled to address outputs of the processor cores wherein the address multiplexor selectively couples one of the processor address outputs to a MUX address output based on the state of the owner signal (MUX_SEL); and a data multiplexor (MUX 46) coupled to data outputs of the processor cores, wherein the data multiplexor selectively couples one of the processor data outputs to a MUX data output based on the state of the owner signal (MUX_SEL).

As to claim 18, Stark further teaches the processor cores comprise embedded processor cores integrated on a single integrated circuit chip (col. 3, lines 53-63 and col. 4, lines 32-57).

As to claim 19, Tanaka further teaches a peripheral control register associated with each of the peripheral units (col. 3, lines 23-43), wherein the peripheral control register is shared amongst the plurality of processors and is integrated on the single integrated circuit chip (as addressed above wherein Stark teaches the system is integrated on a single chip).

10. Claims 20-21 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tanaka (5,408,671) in view of Stirk et al. (5,408,627) (hereinafter Stirk).

As to claim 20, Tanaka disclose a multiprocessor computer system comprising: a pair of processors; an input/output bus connected to the processors; a plurality of peripheral units (registers) connected to the input/output bus (note Fig. 1 for connection between the processors and the peripheral units); coupling each of the plurality of

processors to the shared input/output in response to an owner signal (through access control means 16) (Fig.1, col. 1, lines 50-65, and col. 3, liens 23-68). However, Tanaka does not explicitly disclose a multiplexor for selectably coupling each of the processors to the bus. Stirk teaches multiplexor circuit (Data MUX 46, Address MUX 50, and associated circuits) for coupling each of the processors (A, B, C) to the bus (Figs. 3A-3B and col. 2 line 57 to col. 3 line 44). It would have been obvious to one of ordinary skill in the art at the time the invention was made to include the multiplexor circuitry for coupling each of the of processor to the bus as taught by Stirk in the system of Tanaka to provide efficient accessing to a share resource by a plurality of processors with a low cost (col. 1, lines 13-52) and also to minimize access contention for frequently access of a processor to a particular peripheral unit (by arbitration unit 52).

As to claim 21, Tanaka further teaches a set of peripheral-share registers (in shared register control portion) wherein each member of the set includes an entry associated with each of the plurality of peripheral units holding a state value indicating which of the processors currently owns the associated peripheral unit (Fig.1, col. 1, lines 50-65, and col. 3, liens 23-68).

As to claim 23, Stirk further teaches selective coupling performed by the address multiplexor and by the data multiplexor is based on a state of the owner signal (MUX_SEL) (Figs. 3A-3B and col. 2 line 57 to col. 3 line 44).

11. Claim 22 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tanaka (5,408,671) in view of Stirk et al. (5,408,627) (hereinafter Stirk), and further in view of Starke (5,889,947).

As to claim 22, the argument above for claim 20 applies. However, Tanaka and Stirk do not explicitly disclose the processors comprise embedded processor cores integrated on a single integrated circuit chip. Starke teaches processor cores integrated on a single integrated circuit chip (col. 3, lines 53-63 and col. 4, lines 32-57). It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement processor cores integrated on a single integrated circuit chip as taught by Starke in the system of Tanaka and Stirk to provide greatly increased data bandwidth and decreased latency (col. 3, lines 53-63).

12. Claim 24 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tanaka (5,408,671) in view of Stirk et al. (5,408,627) (hereinafter Stirk), and further in view of Tanaka et al. (6,502,167) (hereinafter Tanaka A.).

As to claim 24, the argument above for claim 20 applies. However, Tanaka and Stirk do not explicitly disclose the system comprises a disk drive controller. Tanaka A. teaches disk drive controller (abstract). It would have been obvious to one of ordinary skill in the art at the time the invention was made to include disk drive controller as taught by Tanaka A. in the system of Tanaka and Stirk to control the transfer of information to and from the memory.

Conclusion

13. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure, as the art discloses multiprocessor system:

US Patent	5,907,862	Smalley
US Patent	5,857,110	Sakakibara et al.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Trisha U. Vu whose telephone number is 703-305-5959. The examiner can normally be reached on Mon-Thur and alternate Fri from 7:00am to 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart can be reached on 703-305-4815. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Trisha Vu

Trisha U. Vu
Examiner
Art Unit 2112

uv

Sumati Lefkowitz

SUMATI LEFKOWITZ
PRIMARY EXAMINER